REMARKS

With this Response, no claims are amended, added, or canceled. Therefore, claims 1-25 are pending.

CLAIM REJECTIONS - 35 U.S.C. § 102

Claims 1-6, 9-11 and 14-22 were rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,835,949 to Quattromani et al. (hereinafter "Quattromani"). Applicant respectfully submits that these claims are not anticipated by the cited reference for at least the following reasons.

Claims 1-6, 9-11, and 14-20

Claim 1 recites the following:

> An instruction memory comprising:
> **memory locations, directly instruction-word-addressable**, to store linear sequences of instruction data in logically contiguous memory locations of increasing logical word address, including instructions that are one or multiple instruction words in size, wherein instructions stored in the memory locations may be fetched in a single instruction cycle;
> memory control logic to indicate a current valid read word address of the memory locations; and
> a permutation unit to receive instruction data read from the memory locations and order the instruction data according to an order of sequential operation.

Claim 9 recites limitations similarly directed to "word-addressable instruction data memory locations." Likewise, claim 14 recites limitations directed to "cache including instruction-word addressable memory locations."

Quattromani fails to disclose or suggest a system for word-addressable instruction data memory locations (as in claims 1, 9, and 14). The system discussed in Quattromani outputs quad-words (meaning a data packet equal in size to four instruction-words) from multiplexers 220 and 222, (Column 8, lines 39-41), which are "sixty-four-bit chunks" (Column 8, line 47). See Quattromani, FIG. 4. Thus as Applicant has understood the reference, the system in Quattromani has 16-bit instruction-words since there are four instruction-words in one quad-word. Additionally, the description of the Quattromani instruction (L0) cache makes no mention of an ability to access an individual instruction-word of instruction data (Columns 9-12). As Applicant has understood the reference, the 16-bit ISA bus in Quattromani's system appears to

pertain not to the passing of *instructions* but *data* to peripherals in contrast to Applicant's system (Column 7, lines 20-25). The Quattromani "microprocessor [only] uses [an] internal thirty-two bit address" bus (Column 4, line 27), and "thirty-two bit registers," (Column 4, line 54), which have the size of double-words further indicating instructions in the system are not handled in a word-addressable fashion. As Applicant has understood the reference, Quattromani fails to consider the use of instruction-word addressable memory locations, in contrast to the claimed invention. Therefore, the reference fails to disclose or suggest at least one element of the claimed invention, and so fails to anticipate the invention as recited in claims 1, 9, and 14.

Claims 2-6, 10-11, and 15-20, rejected under 35 U.S.C. § 102(b), depend from independent claims 1, 9, and 14. As per MPEP § 2143.03 they are therefore not anticipated by the reference for at least the same reasons as set forth with respect to the independent claims.

Claims 21 and 22

Claim 21 recites the following:

> a method comprising:
> **storing units of instruction data in logically sequential memory locations of a level-0 (L0) storage structure**;
> indicating a top-most valid instruction data unit, a bottom-most valid instruction data unit, and a current instruction data unit to execute with pointers;
> reading a number of instruction data units from the L0 storage structure, starting at the memory location of the current instruction data unit pointer; and
> **rearranging** the read instruction data units to align the instruction data units in preparation for execution of an instruction.

Specifically, Claim 21 pertains to *storing* data in *logically sequential* memory locations in a *L0 storage structure* (for example, but not limited to, cache), and then *rearranging* that data upon extraction for execution.

Quattromani fails to disclose or suggest similar methods for data storage and extraction into and out of the L0 storage structure. Quattromani's system only stores data in a sequential manner within a given row, but not across the entire L0 storage structure, contrary to Applicant's system. "[A]ny cache line identified ... as being in either execution pipeline is not replaced," when new data is written to the L0 cache, thus leading to non-sequential storage of data in Quattromani (Column 10, lines 4-13). See also Quattromani, FIG. 6. In Quattromani, sequential data is not necessarily stored in sequential positions in the L0 cache (Columns 11-12). In contrast, Applicant's claim recites storage of instructions in "logically sequential memory

locations" in an L0 storage structure. Moreover, in the claimed invention, the data is rearranged upon extraction when it spans multiple rows of the L0 storage structure. As Applicant has understood the reference, no such rearranging takes place in Quattromani where data-words coming from the L0 cache are simply broken down by multiplexers 224a and 224b and then recombined by multiplexers 220 and 222 without changing their arrangement (Column 8, lines 39-53). Thus, as Applicant has understood the reference, data is *extracted*, not *stored* in the L0 storage structure in a sequential manner, contrary to Applicant's system. Therefore, the reference fails to disclose or suggest at least one element of the claimed invention, and so fails to anticipate the invention as recited in claim 21.

The remaining claim, 22, rejected under 35 U.S.C. § 102(b), depends from independent claim 21. As per MPEP § 2143.03 it is therefore not anticipated by the reference for at least the same reasons as set forth with respect to the independent claim.

CLAIM REJECTIONS - 35 U.S.C. § 103

Claim 7

Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Quattromani as applied to claims 1 and 6 and in further view of US Patent No. 5,418,973 to Ellis et al. (hereinafter "Ellis"). Claim 7 is a dependant claim based on independent claim 1, therefore the prior art references when combined "must teach or suggest all the claim limitations," found in both claims. See MPEP § 2143. The rejection of this claim is based on the same reasoning used to reject claims 1 and 6, discussed above. Applicant respectfully submits that the references both individually and in combination fail to disclose at least the claimed limitation of "memory locations, directly instruction-word-addressable, to store linear sequences of instruction data in logically contiguous memory locations," as cited in claim 1. Whether or not Ellis disclosed the specific elements of claim 7, it fails to cure the deficiencies in claim 1. As per MPEP § 2143.03, claim 7 is nonobvious over the cited reference for at least the same reasons as claim 1. Therefore, Quattromani does not render the claim obvious in further view of Ellis.

Claim 8

Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Quattromani and Ellis as applied to claims 1 and 6-7 and further in view of US Patent No. 5,941,983 to Gupta et al. (hereinafter "Gupta"). Claim 8 is a dependant claim based on independent claim 1,

therefore the prior art references when combined "must teach or suggest all the claim limitations," found in both claims. See MPEP § 2143. The rejection of this claim is based on the same reasoning used to reject claims 1 and 6-7, discussed above. Applicant respectfully submits that the references both individually and in combination fail to disclose at least the claimed limitation of "memory locations, directly instruction-word-addressable, to store linear sequences of instruction data in logically contiguous memory locations," as cited in claim 1. Whether or not Gupta disclosed the specific elements of claim 8, it fails to cure the deficiencies in claim 1. As per MPEP § 2143.03, claim 8 is nonobvious over the cited reference for at least the same reasons as claim 1. Therefore, Quattromani does not render the claim obvious in further view of Gupta.

Claims 12-13

Claims 12-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Quattromani as applied to claims 9 and 11 and further in view of US Patent No. 5,835,949 to Cai et al. (hereinafter "Cai"). Claims 12 and 13 are dependant claims based on independent claim 9, therefore the prior art references when combined "must teach or suggest all the claim limitations," found in all the relevant claims. See MPEP § 2143. The rejection of these claims is based on the same reasoning used to reject claims 9 and 11, discussed above. Applicant respectfully submits that the references both individually and in combination fail to disclose at least the claimed limitation of "word-addressable instruction data memory locations," as cited in claim 9. Whether or not Cai disclosed the specific elements of claims 12 and 13, it fails to cure the deficiencies in claim 9. As per MPEP § 2143.03, claims 12 and 13 are nonobvious over the cited reference for at least the same reasons as claim 9. Therefore, Quattromani does not render the claims obvious in further view of Cai.

Claim 23

Claim 23 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Quattromani as applied to claim 21 and further in view of US Patent No. 6,408,377 B2 to Munson et al. (hereinafter "Munson"). Claim 23 is a dependant claim based on independent claim 21, therefore the prior art references when combined "must teach or suggest all the claim limitations," found in both claims. See MPEP § 2143. The rejection of this claim is based on the same reasoning used to reject claim 21, discussed above. Applicant respectfully submits that the

references both individually and in combination fail to disclose at least the claimed limitation of "storing units of instruction data in logically sequential memory locations of a level-0 (L0) storage structure," as cited in claim 21. Whether or not Munson disclosed the specific elements of claim 23, it fails to cure the deficiencies in claim 21. As per MPEP § 2143.03, claim 23 is nonobvious over the cited reference for at least the same reasons as claim 21. Therefore, Quattromani does not render the claim obvious in further view of Munson.

Claim 24

Claim 24 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Quattromani as applied to claims 21 and 23 and further in view of US Patent Application Publication No. 2005/0147203 A1 to Ross et al. (hereinafter "Ross"). Claim 24 is a dependant claim based on independent claim 21, therefore the prior art references when combined "must teach or suggest all the claim limitations," found in both claims. See MPEP § 2143. The rejection of this claim is based on the same reasoning used to reject claim 21, discussed above. Applicant respectfully submits that the references both individually and in combination fail to disclose at least the claimed limitation of "storing units of instruction data in logically sequential memory locations of a level-0 (L0) storage structure," as cited in claim 21. Whether or not Ross disclosed the specific elements of claim 24, it fails to cure the deficiencies in claim 21. As per MPEP § 2143.03, claim 24 is nonobvious over the cited reference for at least the same reasons as claim 21. Therefore, Quattromani does not render the claim obvious in further view of Ross.

Claim 25

Claim 25 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Quattromani as applied to claims 21 and 23-24 and further in view of US Patent No. 5,239,584 to Hershey et al. (hereinafter "Hershey"). Claim 25 is a dependant claim based on independent claim 21, therefore the prior art references when combined "must teach or suggest all the claim limitations," found in both claims. See MPEP § 2143. The rejection of this claim is based on the same reasoning used to reject claim 21, discussed above. Applicant respectfully submits that the references both individually and in combination fail to disclose at least the claimed limitation of "storing units of instruction data in logically sequential memory locations of a level-0 (L0) storage structure," as cited in claim 21. Whether or not Hershey disclosed the specific elements of claim 25, it fails to cure the deficiencies in claim 21. As per MPEP § 2143.03, claim 25 is

nonobvious over the cited reference for at least the same reasons as claim 21. Therefore, Quattromani does not render the claim obvious in further view of Hershey.

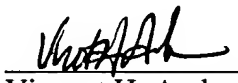
CONCLUSION

For at least the foregoing reasons, Applicant submits that the rejections of the claims have been overcome herein, placing all pending claims in condition for allowance. Such action is earnestly solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the above-referenced application.

Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

Date: June 15, 2006



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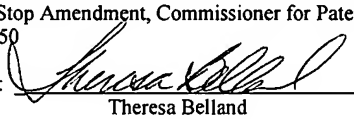
Signature:  06/15/06
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